What is claimed is:

1. An apparatus comprising:

multiprocessing circuitry to execute a plurality of processes;

causality monitoring logic to transparently monitor potential causal relationships with respect to stores observed by one or more of the plurality of processes; and

arbitration logic coupled with the causality monitoring logic to allow a plurality of stores generated in a first order of stores by two or more of the plurality of processes to be observed by at least one of the plurality of processes, the observation by said at least one of the plurality of processes indicating an order of stores different from the first order of stores.

2. The apparatus of claim 1 wherein said apparatus is integrated into a single multiprocessing integrated circuit.

3. The apparatus of claim 2 wherein the arbitration logic is a first switch-based arbitration logic coupled to at least one memory or another switch-based arbitration logic.

4. The apparatus of claim 1 further comprising:

buffering circuitry, said causality monitoring logic being coupled with said buffering circuitry to monitor potential causal relationships with respect to

buffered stores.

5. The apparatus of claim 4 wherein said causality monitoring logic is to set one or more ordering bits to indicate an ordering restriction in said buffering circuitry to prevent a reordering of stores if the reordering would violate a potential causality relationship with respect to a store observed by one or more of said plurality of processes.

6. The apparatus of claim 1 further comprising:

store forwarding logic coupled with the causality monitoring logic to signal a potential causal relationship being established when data is forwarded from a first store to a first memory location from a first one of said plurality of processes to a load of the first memory location from a second one of said plurality of processes when a prior potential causal relationship does not exist.

7. An apparatus comprising:

a plurality of processors;

access optimization buffering circuitry;

causality monitoring logic to monitor causal relationships with respect to observed stores; and

arbitration logic coupled with the causality monitoring logic and said access optimization buffering circuitry and to allow a plurality of stores generated in a first order of stores by any two or more of the plurality of processors

to be observed by at least one of said plurality of processors, wherein the observation indicates an order of stores different from said first order of stores.

8. The apparatus of claim 7 wherein said apparatus is integrated into a single multiprocessing integrated circuit.

9. The apparatus of claim 7 wherein the arbitration logic is switch-based arbitration logic individually coupled to each of said plurality of processors and to at least one memory or another switch-based arbitration logic.

10. The apparatus of claim 7 wherein said causality monitoring logic is coupled with said access optimization buffering circuitry to monitor causal relationships with respect to buffered stores.

11. The apparatus of claim 10 wherein said causality monitoring logic is to set an ordering restriction in said access optimization buffering circuitry to prevent a reordering of one of the plurality of stores if the reordering would violate causality with respect to any observed stores.

12. The apparatus of claim 7 further comprising:

store forwarding logic coupled with the causality monitoring logic to signal a causal relationship being established when data is forwarded from a first

store to a first memory location from a first one of said plurality of processors to a load of the first memory location from a second one of said plurality of processors when a prior causal relationship does not exist.

13. A machine automated method comprising:

receiving a plurality of stores generated in a first order of stores from a plurality of bus agents;

allowing the plurality of stores to be observed by at least one other of said plurality of bus agents, said observation contradicting the first order of stores;

dynamically determining if causality with respect to observed stores would be violated by allowing the plurality of stores to be observed contradictory with the first order of stores; and

maintaining a processor consistency memory ordering model transparently to said plurality of bus agents.

14. The machine automated method of claim 13 further comprising:

preventing a reordering of any one of the plurality of stores if the reordering would violate causality with respect to observed stores; and

reordering a subset of the plurality of stores that does not violate causality with respect to observed stores to be observed contradictory with the first order of stores by at least one of said plurality of bus agents.

15. The machine automated method of claim 14 wherein preventing comprises setting one or more ordering bits in a store buffer to indicate an ordering restriction.

16. The machine automated method of claim 13 further comprising:

ensuring that stores from any one of the plurality of bus agents are observed, consistent with the first order of said stores by all of said plurality of bus agents.

17. A system comprising:

a plurality of processors;

store buffering circuitry to buffer stores received from at least one processor of the plurality of processors;

causality monitoring logic coupled to said store buffering circuity, the causality monitoring logic to monitor, for said plurality of processors, causal relationships with respect to buffered stores; and

store forwarding logic to forward data from a first store to a first memory location from a first one of said plurality of processors to a load of the first memory location from a second one of said plurality of processors if no causal relationship exists with respect to the first store and the second one of said plurality of processors.

18. The system of claim 17 wherein said causality monitoring logic is to set one or more

ordering bits to indicate an ordering restriction in said store buffering circuitry to prevent a reordering one of the plurality of stores if the reordering would violate causality with respect to observed stores.

19. The system of claim 17 wherein said causality monitoring logic is to record a causal relationship between the first store to memory and a second store to memory from said second one of said plurality of processors when said first one of said plurality of processors observes the second store to memory prior to generating the first store to memory or when said second one of said plurality of processors observes the first store to memory prior to generating the second store to memory.

20. The system of claim 17 wherein said causality monitoring logic is to record a causal relationship being established when data is forwarded from the first store to the first memory location from said first one of said plurality of processors to the load of the first memory location from said second one of said plurality of processors when a prior causal relationship does not exist.